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J Cong, S Xu - PROC DES AUTOM CONF. pp. 704-707. 1998, 1998 - [ieeexplore.ieee.org](#)

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J Cong, S Xu - IEEE ACM INT CONF COMPUT AIDED DES DIG TECH PAP. pp. 40-45. ..., 1998 - [cs.ucla.edu](#)... Jason Cong and Songjie Xu Computer Science Department University of California, Los Angeles, CA 90095 [cong@cs.ucla.edu](#) [sxu@cs.ucla.edu](#) [http://cadlab.cs.ucla.edu](#) ...Cited by 8 - [View as HTML](#) - [Web Search](#) - [portal.acm.org](#) - [ieeexplore.ieee.org](#) - [csa.com](#) - [all 5 versions »](#)

### Synthesis Challenges for Next-Generation High-Performance and High-Density PLDs

J Cong, S Xu - Asia and South Pacific Design Automation Conf., January, 2000 - [ieeexplore.ieee.org](#)... 24.50% Songjie Xu Aplus Design Technologies, Inc. 10850 Wilshire Blvd., Suite 370, Los Angeles, CA 90024, USA [sxu@aplus-dt.com](#) LSI Logic Abstract ...Cited by 6 - [Web Search](#) - [portal.acm.org](#) - [portal.acm.org](#) - [ieeexplore.ieee.org](#)

### Technology mapping for FPGAs with nonuniform pin delays and fast interconnections

J Cong, YY Hwang, S Xu - PROC DES AUTOM CONF. pp. 373-378. 1999, 1999 - [ieeexplore.ieee.org](#)... Jason Cong, Yean-Yow Hwang and Songjie Xu Department of Computer Science University of California, Los Angeles, CA 90095 { cong, yeanyow, sxu } [@cs.ucla.edu](#) ...Cited by 4 - [Web Search](#) - [portal.acm.org](#) - [portal.acm.org](#) - [csa.com](#) - [all 5 versions »](#)

### Performance-Driven Technology Mapping for Heterogeneous FPGAs

JJ Cong, S Xu - IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED ..., 2000 - [ieeexplore.ieee.org](#)

... 19, NO. 11, NOVEMBER 2000 Performance-Driven Technology Mapping for Heterogeneous FPGAs Jingsheng Jason Cong, Senior Member, IEEE and Songjie Xu, Member, IEEE ...

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### Exact tree-based FPGA technology mapping for logic blocks with independent LUTs

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Combining technology mapping and placement for delay-optimization in FPGA designs.

CS Chen, YW Tsay, TT Hwang, ACH Wu, YL Lin - 1993 - [portal.acm.org](http://portal.acm.org)

... Jason Cong , **Songjie Xu**, Invited talk: synthesis challenges for next-generation high-performance and high-density PLDs, Proceedings on the 2000 conference on ...

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DAG-Map: Graph-Based FPGA Technology Mapping for Delay Optimization

KC Chen, J Cong, Y Ding, AB Kahng, P Trajmar - IEEE Design & Test, 1992 - [portal.acm.org](http://portal.acm.org)

... Jason Cong , **Songjie Xu**, Delay-optimal technology mapping for FPGAs with heterogeneous LUTs, Proceedings of the 35th annual conference on Design automation ...

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